CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). In a computer system having a plurality of processor boards, each of the processor boards generating a plurality of error signals in response to different conditions on the processor boards, and a parallel transaction bus connected to each of the processor boards, an error reporting network comprising:

a signal line, separate from the parallel transaction bus, and connected to each of the processor boards; and

each of the processor boards containing:

means for generating an error detection signal;

control means responsive to the error detection signal for generating in sequence a plurality of control signals;

means responsive to one of the control signals for collecting and storing the plurality of error signals;

means responsive to one of the control signals for generating an error notification signal and for communicating the error notification signal to each of the processor boards over said signal line; ~~and~~

means responsive to one of the control signals for communicating the plurality of error signals to each of the processor boards serially over said signal line;

storage means;

further control means responsive to the error notification signal for generating in sequence a plurality of further control signals;

means responsive to one of the further control signals for converting to parallel form and storing in said storage means as error information the plurality of error signals communicated from each of the processor boards serially over said signal line; and

means connected to said storage means for reading out the error information.

Claim 2 (cancelled).

Claim 3 (currently amended). The network according to ~~claim 2~~ claim 1, wherein each of the processor boards is assigned a different slot number and said signal line is time division multiplexed between all of the processor boards, and said control means being responsive to the slot number for controlling said means for communicating so as to communicate the plurality of error signals serially over said signal line within a predetermined time slot in relation to other ones of the processor boards.

Claim 4 (currently amended). A method of communicating an error status between processor boards of a computer system, each of the processor boards generating a plurality of error signals in response to different conditions on the processor boards, the computer system further having a parallel transaction bus connected to each of the processor boards, and a signal line, separate from the parallel transaction bus, connected to each of the processor boards, each of the processor boards performing the steps of:

generating an error detection signal;

generating in sequence a plurality of control signals;

collecting and storing the plurality of error signals;

generating an error notification signal and communicating the error notification signal to each of the processor boards over the signal line; ~~and~~

communicating the plurality of error signals to each of the processor boards serially over the signal line;

generating in sequence a plurality of further control signals in response to the error notification signal;

converting to parallel form and storing as error information the plurality of error signals communicated from each of the processor boards serially over the signal line; and

reading out the error information.

Claim 5 (cancelled).

Claim 6 (currently amended). The method according to ~~claim 5~~ claim 4, which further comprises:

assigning each of the processor boards a different slot number and the signal line is time division multiplexed between all of the processor boards; and

during the communicating step, communicating the plurality of error signals serially over the signal line within a predetermined time slot in relation to other ones of the processor boards.

Claim 7 (currently amended). A computer system, comprising:

a plurality of processor boards each generating a plurality of error signals in response to different conditions on said processor boards;

a parallel transaction bus connected to each of said processor boards; and

a signal line, separate from said parallel transaction bus, and connected to each of said processor boards;

each of said processor boards containing:

means for generating an error detection signal;

control means responsive to the error detection signal for generating in sequence a plurality of control signals;

means responsive to one of the control signals for collecting and storing the plurality of error signals;

means responsive to one of the control signals for generating an error notification signal and for communicating the error notification signal to each of said processor boards over said signal line; ~~and~~

means responsive to one of the control signals for communicating the plurality of error signals to each of said processor boards serially over said signal line;

storage means;

further control means responsive to the error notification signal for generating in sequence a plurality of further control signals;

means responsive to one of the further control signals for converting to parallel form and storing in said storage means as error information the plurality of error signals communicated from each of said processor boards serially over said signal line; and

means connected to said storage means for reading out the error information.

Claim 8 (cancelled).

Claim 9 (original). The computer system according to claim 7, wherein each of said processor boards is assigned a different slot number and said signal line is time division multiplexed between all of said processor boards, and said control means being responsive to the slot number for controlling said means for

communicating so as to communicate the plurality of error signals serially over said signal line within a predetermined time slot in relation to other ones of said processor boards.

Claim 10 (currently amended). A computer system, comprising

a plurality of processor boards generating a plurality of error signals in response to different conditions on said processor boards;

a parallel transaction bus connected to each of said processor boards; and

a signal line, separate from said parallel transaction bus, connected to each of said processor boards;

each of said processor boards communicating an error status between said processor boards by being programmed to:

generate an error detection signal;

generate in sequence a plurality of control signals;

collect and store the plurality of error signals;

generate an error notification signal and communicate the error notification signal to each of said processor boards over said signal line; ~~and~~

communicate the plurality of error signals to each of said processor boards serially over said signal line;

generate in sequence a plurality of further control signals in response to the error notification signal;

convert to parallel form and store as error information the plurality of error signals communicated from each of said processor boards serially over said signal line; and

read out the error information.

Claim 11 (cancelled).

Claim 12 (original). The computer system according to claim 11, wherein said processor boards further programmed to:

assign each of said processor boards a different slot number and said signal line is time division multiplexed between all of said processor boards; and

communicate the plurality of error signals serially over said signal line within a predetermined time slot in relation to other ones of said processor boards.